Engr433 : Digital Design

Registers and Counters

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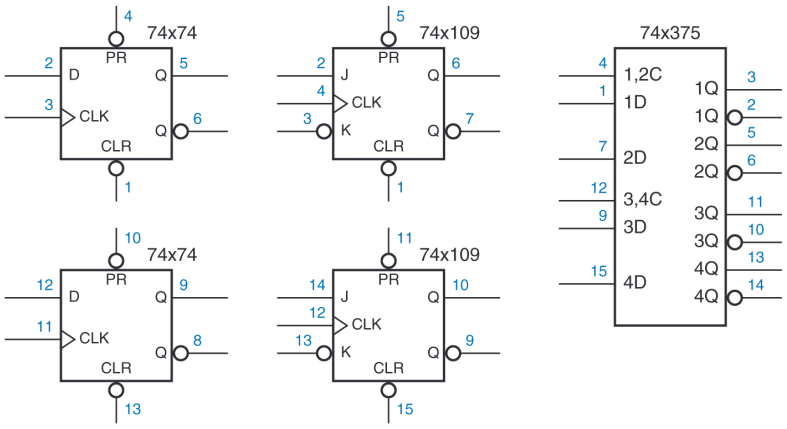
Overview

- In this presentation we cover:
  - Registers, which store multiple bits;
  - Shift registers, which shift the contents of registers;
  - Counters of various types.

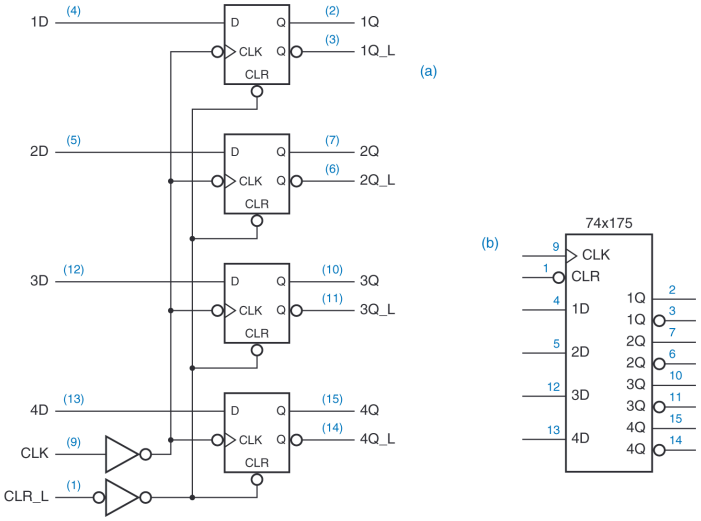
Review - Sequential Circuits

- ***Combinational*** – outputs depends only on the inputs;
- ***Sequential*** – output depends on input and past behavior:
  - Requires use of storage elements;
  - Content of the storage elements is called *state;*
  - Circuit goes through a sequence of states as a result of changes in inputs.
- ***Synchronous*** – Controlled by a clock;
- ***Asynchronous*** – No central clock.

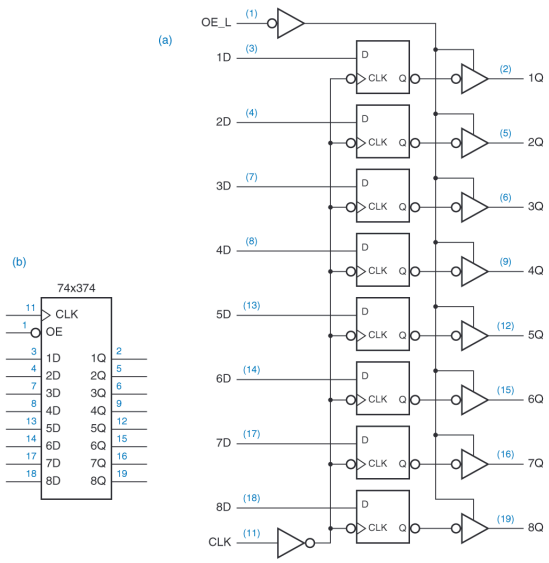
Latches and Flip-Flops



Multibit Registers and Latches

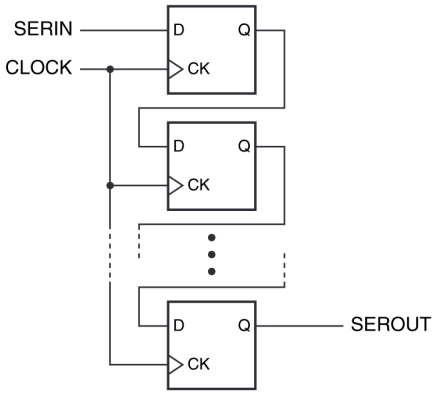


74x374 8-bit Register

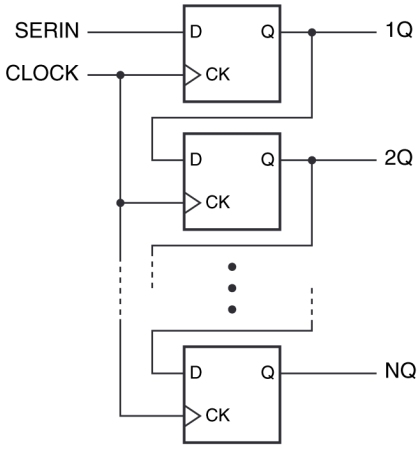


Shift Registers

- A *shift register* is an n-bit register with a provision for shifting stored data by one bit position at each tick of the clock.



Shift Registers – Serial-in, Parallel-out



74x194 4-bit Universal Shift Register

Function	Inputs		Next state			
	S1	S0	QA*	QB*	QC*	QD*
Hold	0	0	QA	QB	QC	QD
Shift right	0	1	RIN	QA	QB	QC
Shift left	1	0	QB	QC	QD	LIN
Load	1	1	A	B	C	D

Table 8-24

Function table for the 74×194 4-bit universal shift register.

74x194 4-bit Universal Shift Register

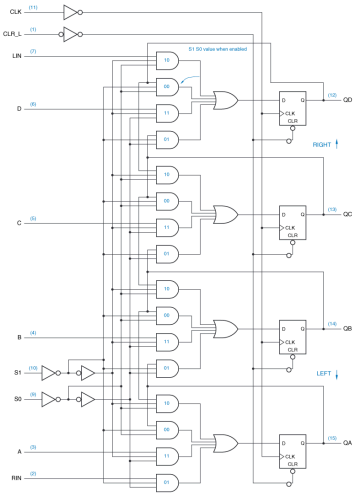


Figure 8-41

Logic diagram for the 74×194 4-bit universal shift register, including pin numbers for a standard 16-pin dual in-line package.

74x194 4-bit Universal Shift Register

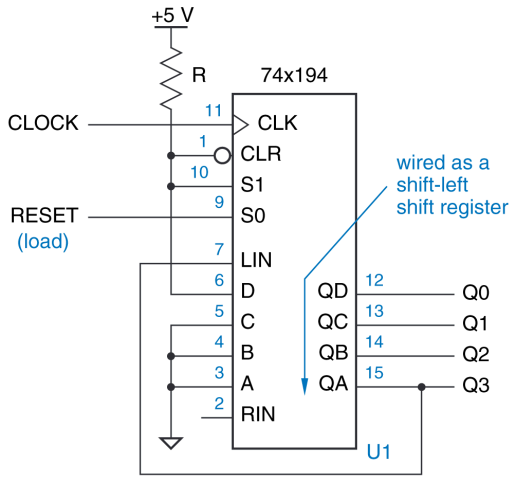


Figure 8-42

Simplest design for a 4-bit, 4-state ring counter with a single circulating 1.

74x194 4-bit Universal Shift Register

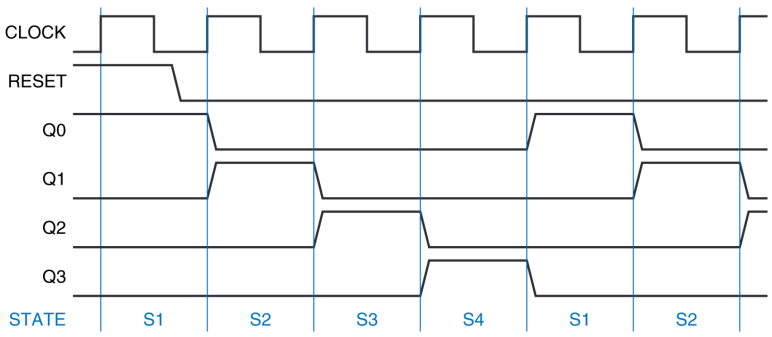
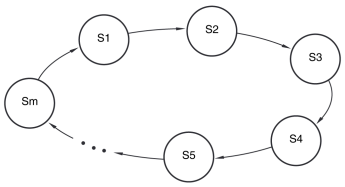


Figure 8-43

Timing diagram for a 4-bit ring counter.

Counters

- *Counter* – generally used for any clocked sequential circuit whose state diagram contains a single cycle;
- *Modulus* – the number of states in the cycle;
- A counter with m states is called a *modulus-m* counter or a *divide-by-m* counter;
- *Ripple* counters (rare due to delays);
- *Synchronous* counters (common):
  - Connects all of its flip-flop clock inputs to the same common *CLK* signal so that all flip-flop outputs change at the same time.



Synchronous 4-bit Binary Counter – 74x163

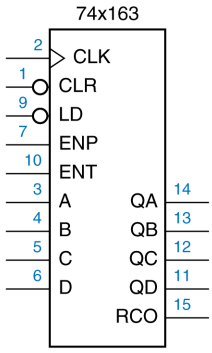


Figure 8-27
Traditional logic symbol for the 74×163.

Inputs				Current State				Next State			
CLR_L	LD_L	ENT	ENP	QD	QC	QB	QA	QD*	QC*	QB*	QA*
0	x	x	x	x	x	x	x	0	0	0	0
1	0	x	x	x	x	x	x	D	C	B	A
1	1	0	x	x	x	x	x	QD	QC	QB	QA
1	1	x	0	x	x	x	x	QD	QC	QB	QA
1	1	1	1	0	0	0	0	0	0	0	1
1	1	1	1	0	0	0	1	0	0	1	0
1	1	1	1	0	0	1	0	0	0	1	1
1	1	1	1	0	0	1	1	0	1	0	0
1	1	1	1	0	1	0	0	0	1	0	1
1	1	1	1	0	1	0	1	0	1	1	0
1	1	1	1	0	1	1	0	0	1	1	1
1	1	1	1	0	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0	1	0	0	1
1	1	1	1	1	0	0	1	1	0	1	0
1	1	1	1	1	0	1	0	1	0	1	1
1	1	1	1	1	0	1	1	1	1	0	0
1	1	1	1	1	1	0	0	1	1	0	1
1	1	1	1	1	1	0	1	1	1	1	0
1	1	1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1	0	0	0	0

Table 8-13
State table for a 74×163 4-bit binary counter.

Synchronous 4-bit Binary Counter – 74x163

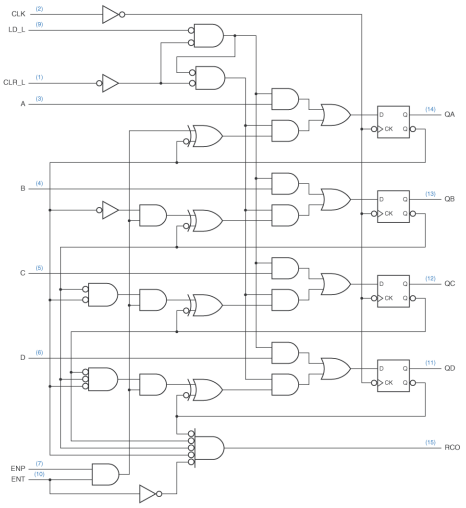


Figure 8-28

Logic diagram for the 74×163 synchronous 4-bit binary counter, including pin numbers for a standard 16-pin DIP package.

Synchronous 4-bit Binary Counter – 74x163

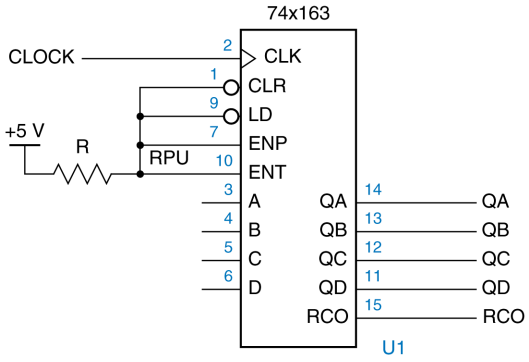


Figure 8-29

Connections for the 74×163 to operate in a free-running mode.

Synchronous 4-bit Binary Counter – 74x169

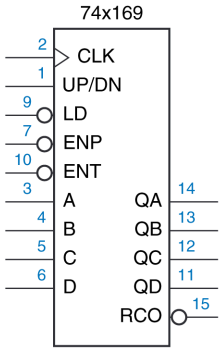
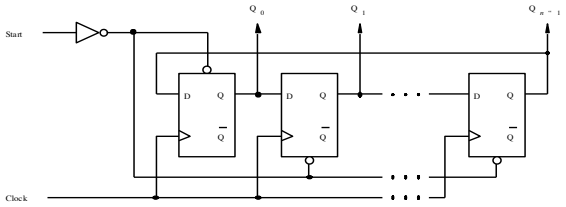
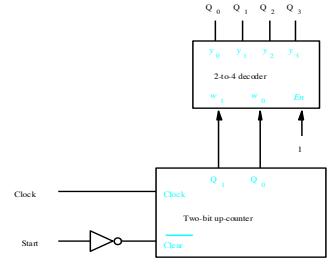


Figure 8-32
Logic symbol for the 74×169 up/down counter.

Ring Counter

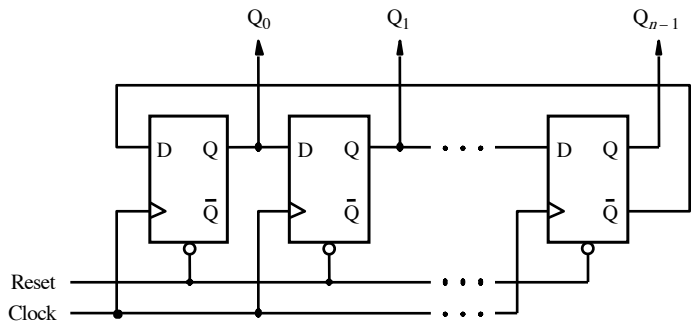


(a) An *n*-bit ring counter

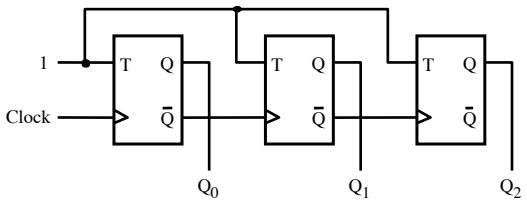


(b) A four-bit ring counter

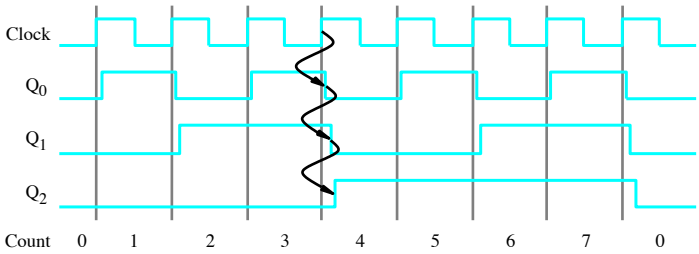
Johnson Counter



Three-Bit Up-Counter

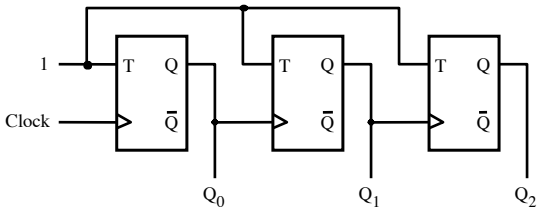


(a) Circuit

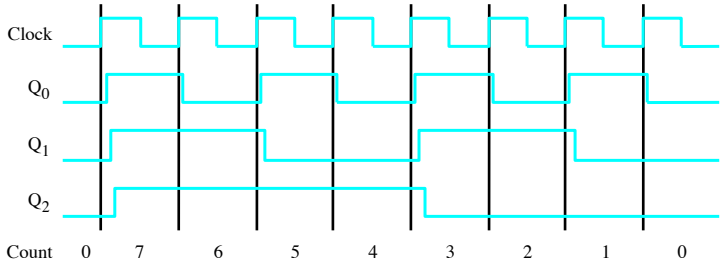


(b) Timing diagram

Three-bit Down-Counter

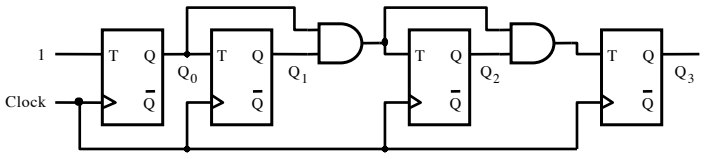


(a) Circuit

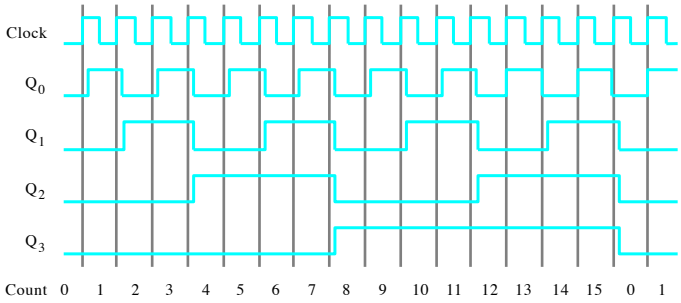


(b) Timing diagram

Four-bit Synchronous Up-Counter

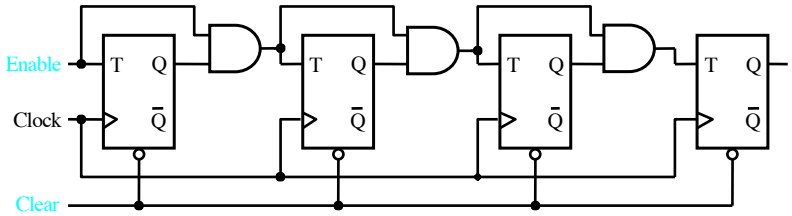


(a) Circuit

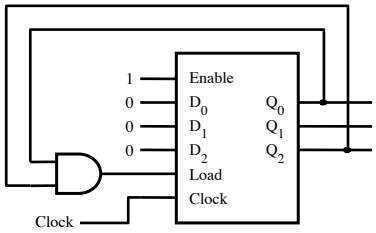


(b) Timing diagram

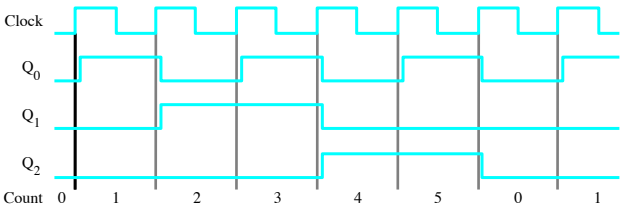
Inclusion of Enable and Clear Capability



Modulo-6 Counter with Synchronous Reset

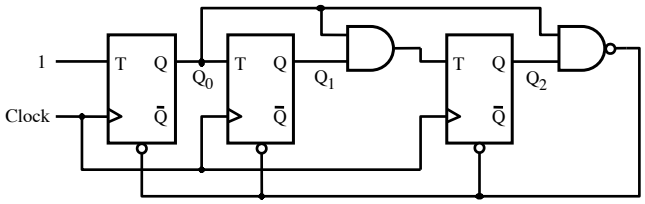


(a) Circuit

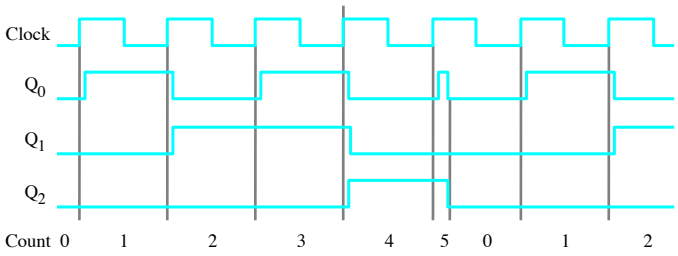


(b) Timing diagram

Modulo-6 Counter with Asynchronous Reset

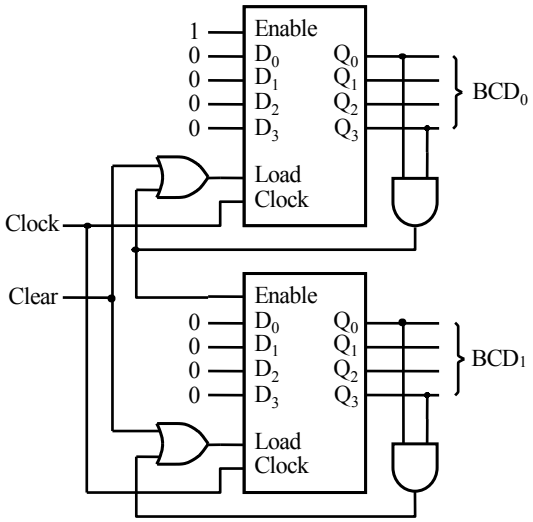


(a) Circuit



(b) Timing diagram

A Two-digit BCD Counter



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